

FIG. 1

TITLE: METHOD AND APPARATUS FOR REALIGNING BITS ON A PARALLEL BUS
INVENTOR(S) NAME: MATTHEW HAYCOCK ET AL.
DOCKET NO.: 884.455US1

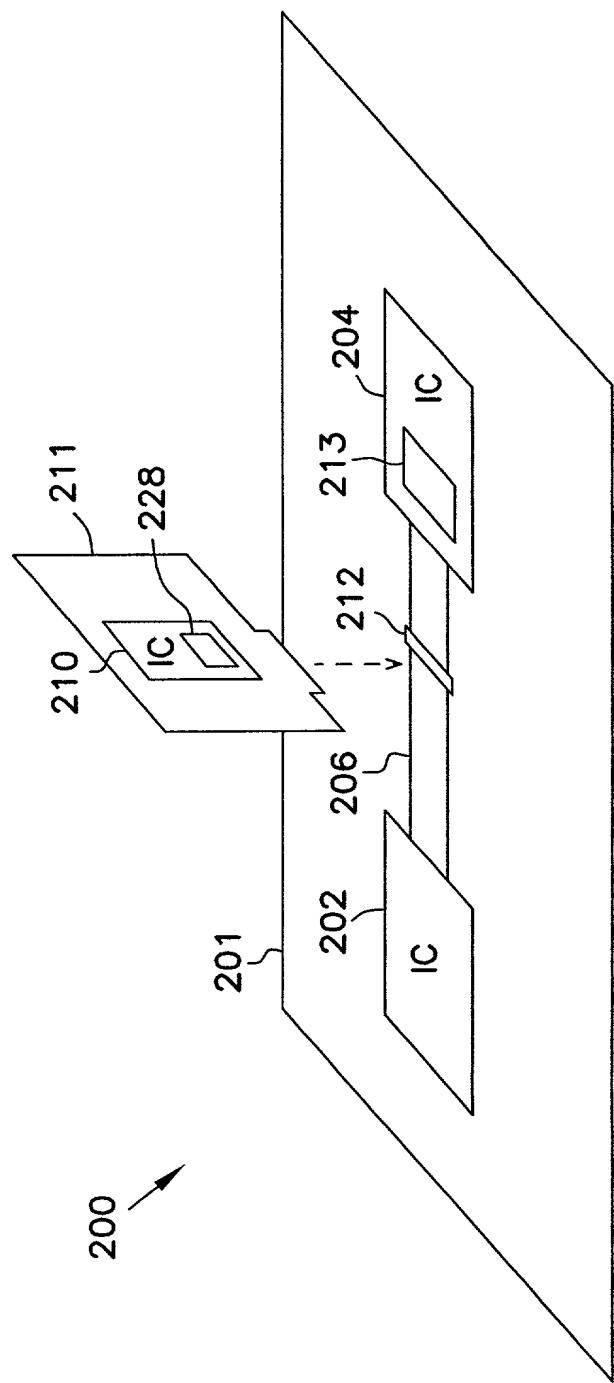


FIG. 2

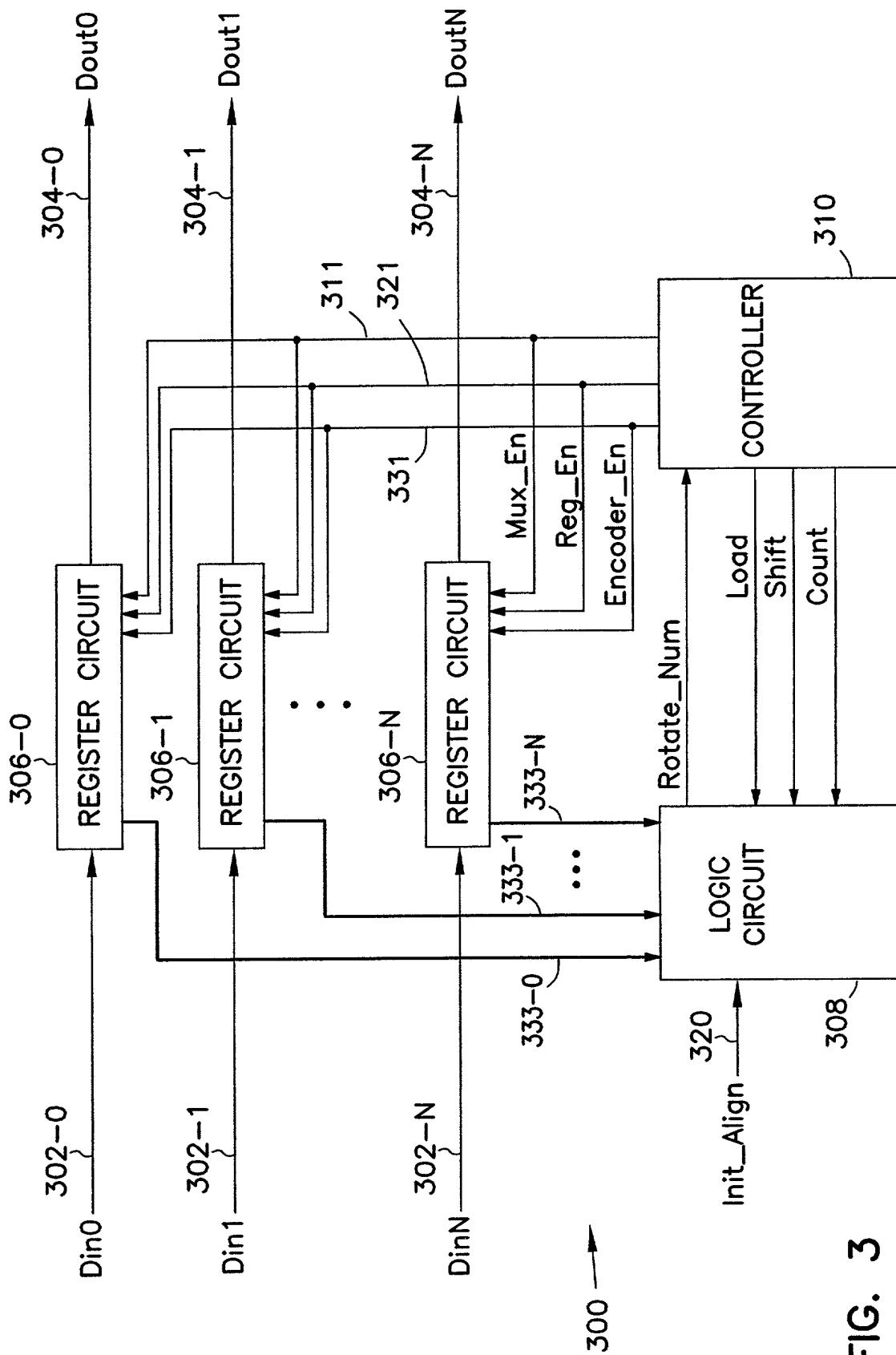
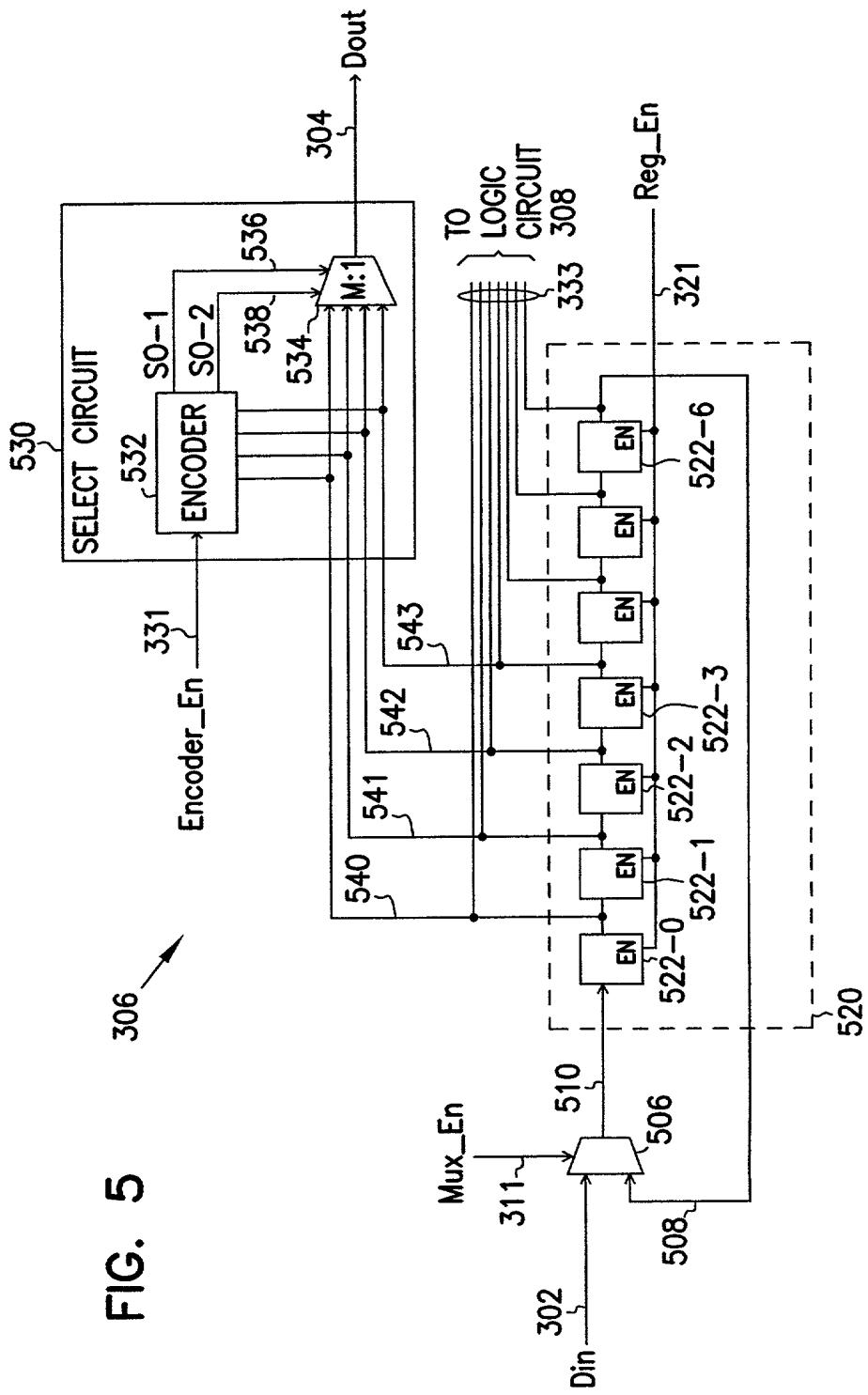


FIG. 3

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TRANSMITTED BITS: 1000010000			
DATA BIT #	RECEIVED AT 302 0-N	OUTPUT AT 304 0-N	
0	1000010000	1000010000	
1	0100001000	1000010000	
...	
N	0010000100	1000010000	

FIG. 4



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TRAINING PATTERNS: 100000010000001000000...	
RECEIVED PATTERNS:	
AT 1ST INPUT	 100000010000001000000...
AT 2ND INPUT	010000001000000100000...
AT 3RD INPUT	001000000100000010000...
AT 4TH INPUT	100000010000001000000...

FIG. 6

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CONTENTS OF:	
REGISTER 700	1000000
REGISTER 701	0100000
REGISTER 702	0000001
REGISTER 703	1000000
	{ 7 BIT TIME INTERVALS }

FIG. 7A

CONTENTS OF:	
REGISTER 700	0100000
REGISTER 701	0010000
REGISTER 702	1000000
REGISTER 703	0100000
	{ 3 BIT TIME INTERVALS }

FIG. 7B

CONTENTS OF:	COLUMN 0	COLUMN 6
REGISTER 800	1000000	
REGISTER 801	0100000	
REGISTER 802	0000001	
REGISTER 803	1000000	
BIT-WISE OR		1100001 (RESULTANT LOGIC VECTOR)

FIG. 8A

ROW	ARRAY 1100001 (RESULTANT LOGIC VECTOR)
0	1100000
1	0111000
2	0011100
3	0001110
4	0000111
5	1000011
6	

FIG. 8B

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BEFORE ROTATION

REGISTER 700	1000000
REGISTER 701	0100000
REGISTER 702	0000001
REGISTER 703	1000000

FIG. 9A

AFTER ONE ROTATION

REGISTER 700	0100000
REGISTER 701	0010000
REGISTER 702	1000000
REGISTER 703	0100000

FIG. 9B

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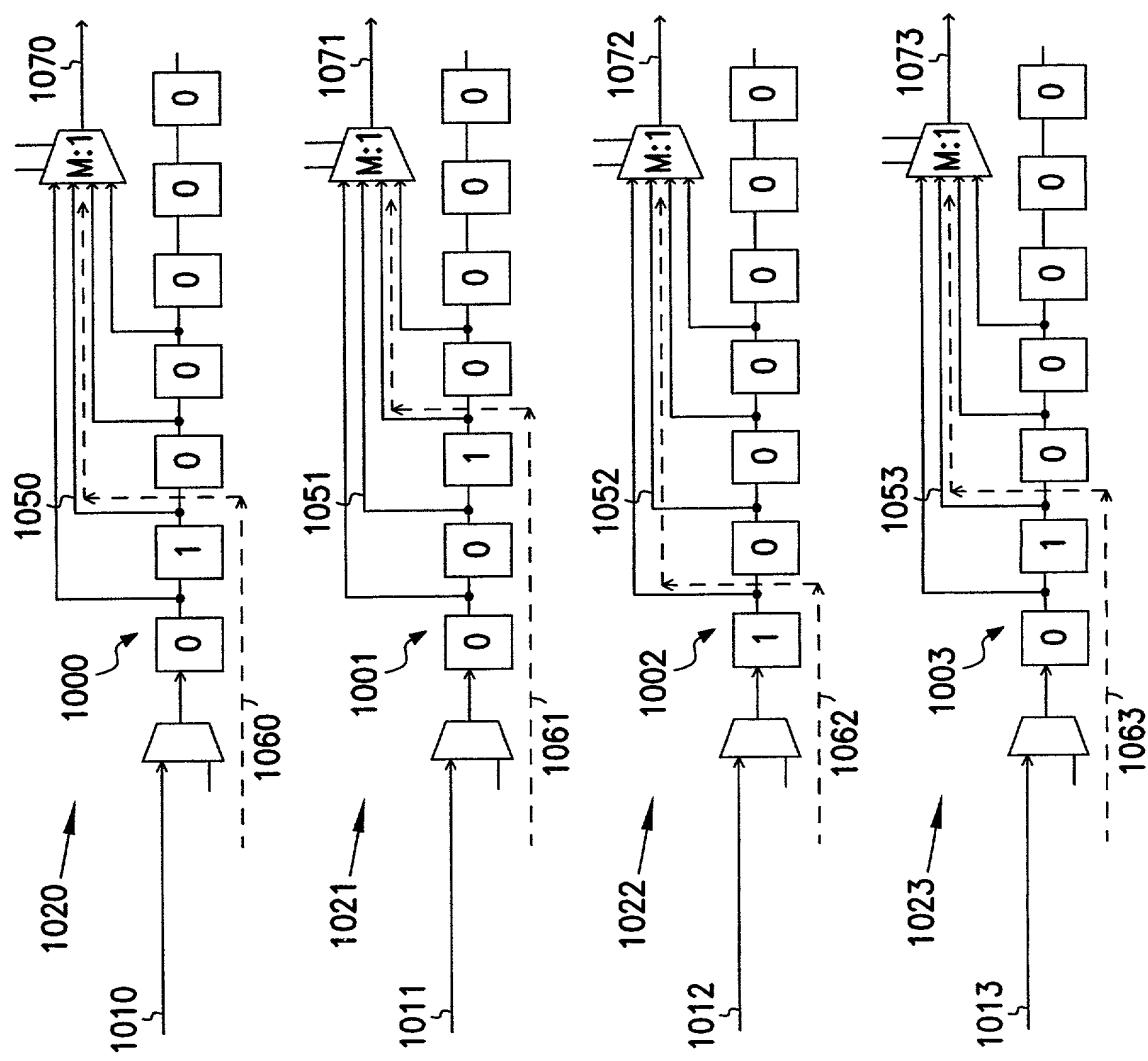
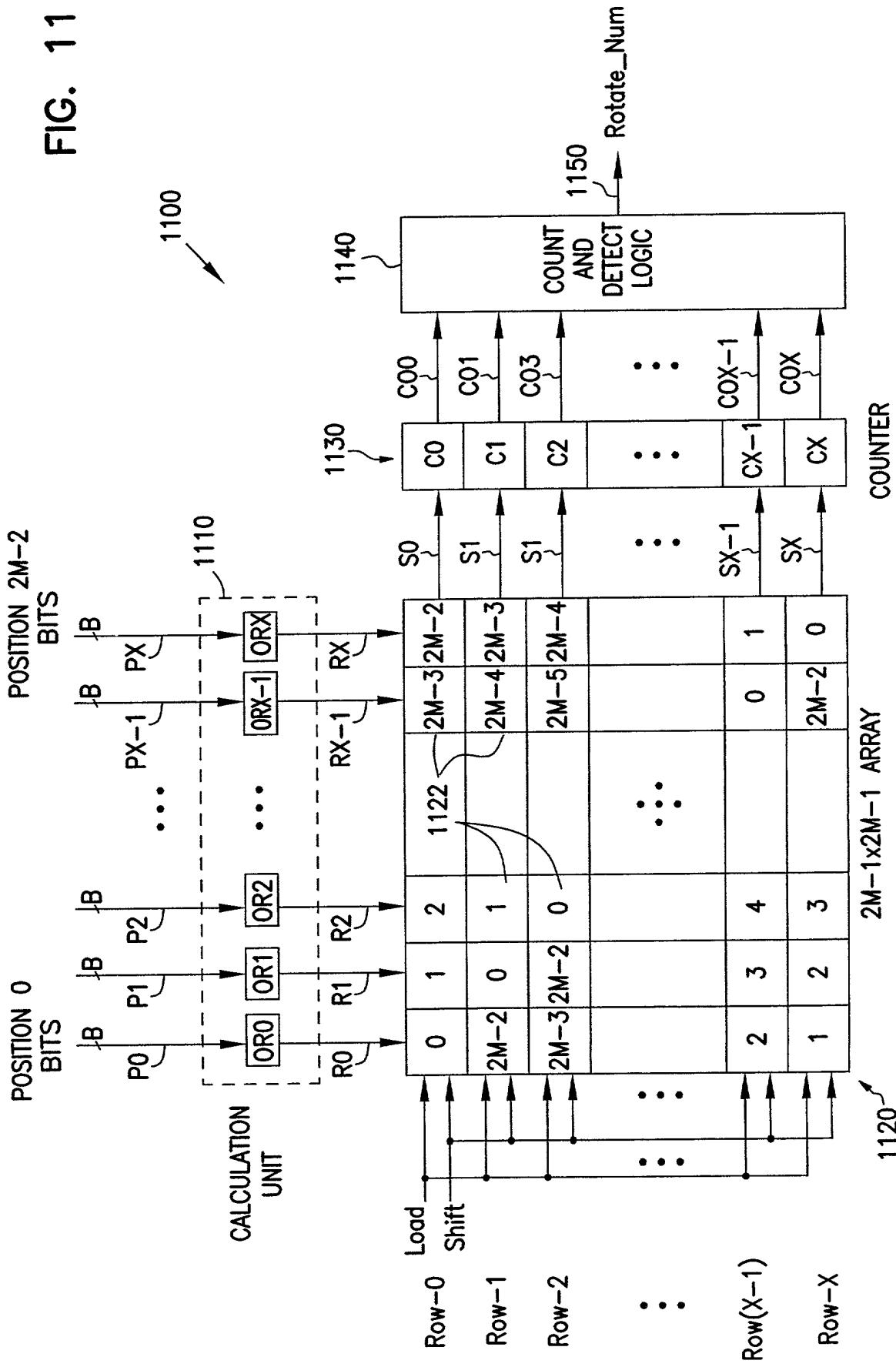


FIG. 10

FIG. 11



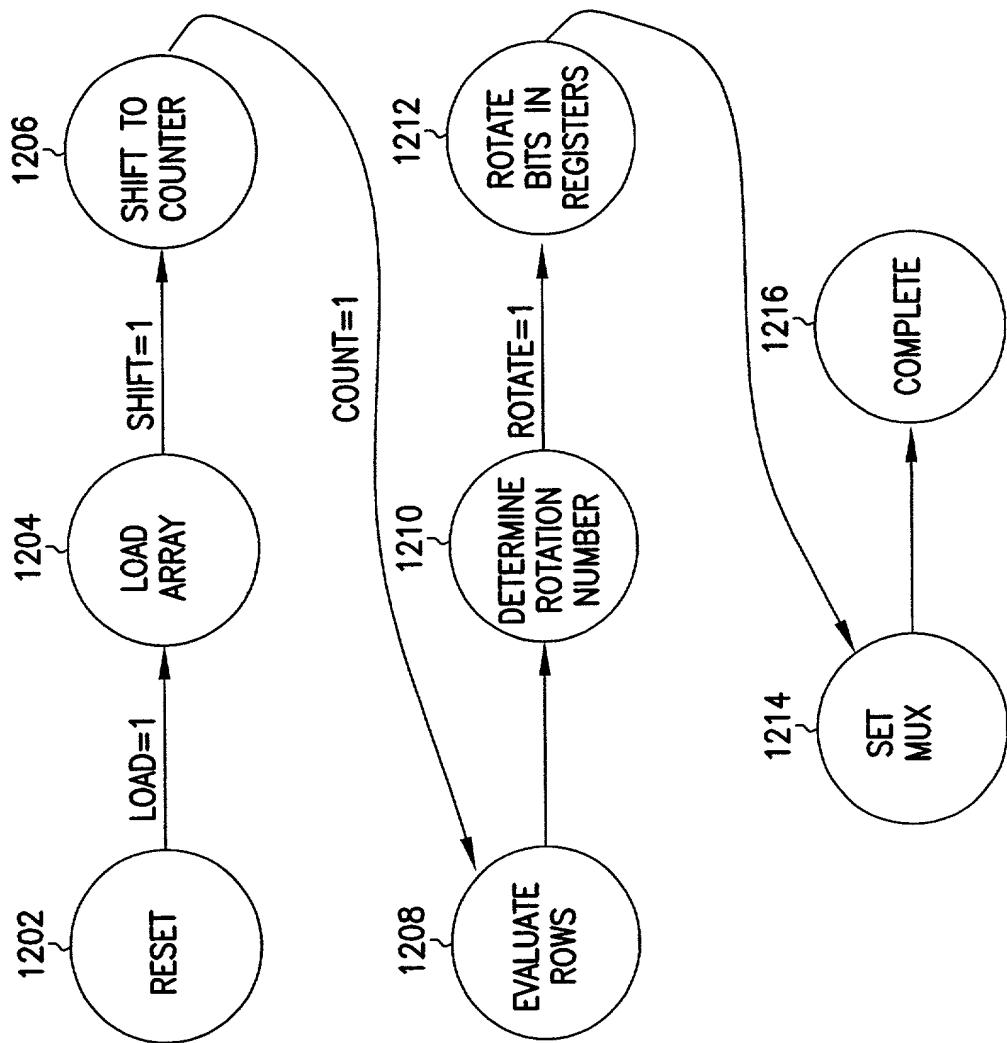


FIG. 12

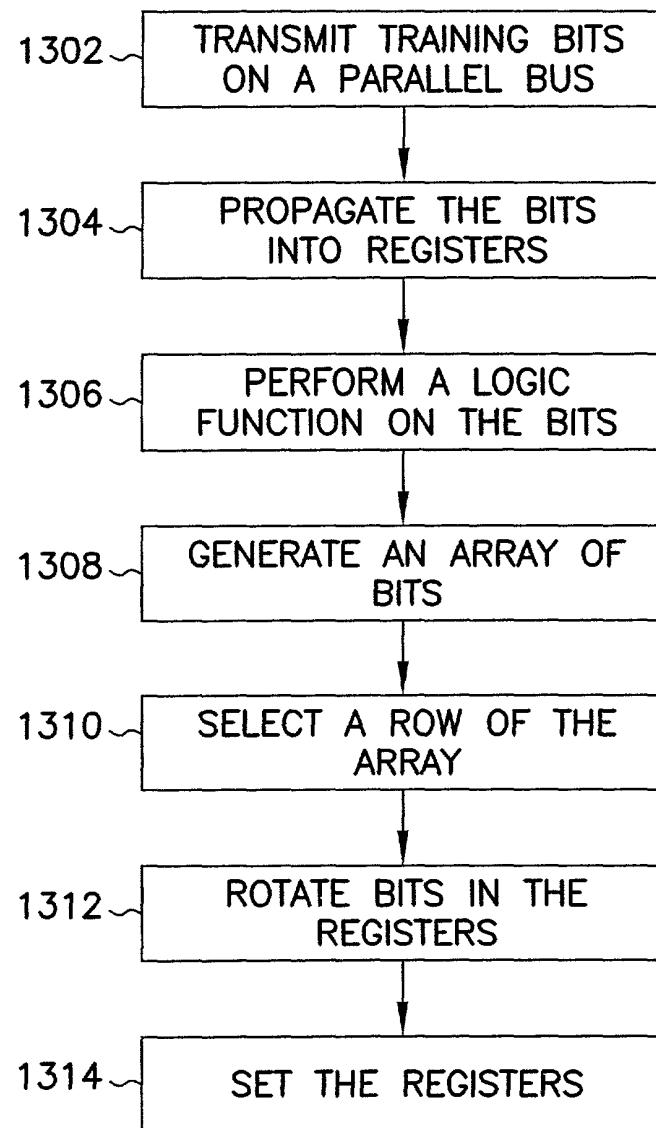


FIG. 13